[Delta] IDDQ testing of a CMOS 12-bit charge scaling digital-to-analog converter

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ΔI_{DDQ} TESTING OF A CMOS 12-BIT CHARGE SCALING DIGITAL-TO-ANALOG CONVERTER

A Thesis

Submitted to the Graduate Faculty of the Louisiana State University and Agricultural and Mechanical College in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

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The Department of Electrical and Computer Engineering

by
Kalyan Madhav Golla
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ABSTRACT

This work presents design, implementation and test of a built-in current sensor (BICS) for ΔI_{DDQ} testing of a CMOS 12-bit charge scaling digital-to-analog converter (DAC). The sensor uses power discharge method for the fault detection. The sensor operates in two modes, the test mode and the normal mode. In the test mode, the BICS is connected to the circuit under test (CUT) which is DAC and detects abnormal currents caused by manufacturing defects. In the normal mode, BICS is isolated from the CUT. The BICS is integrated with the DAC and is implemented in a 0.5 µm n-well CMOS technology. The DAC uses charge scaling method for the design and a low voltage (0 to 2.5 V) folded cascode op-amp. The built-in current sensor (BICS) has a resolution of 0.5 µA. Faults have been introduced into DAC using fault injection transistors (FITs). The method of ΔI_{DDQ} testing has been verified both from simulation and experimental measurements.
CHAPTER 1
INTRODUCTION

$\text{I}_{\text{DDQ}}$ testing is a method for testing VLSI circuits by detecting elevated levels of quiescent current (steady state current) caused by defects in the circuit [1,2]. Traditionally $\text{I}_{\text{DDQ}}$ is measured on a set of test vectors and the maximum measured current from the set is compared to a threshold value. If the maximum measured current is higher than the threshold, the test fails; if the measured current is below the threshold the test passes. This method of testing of CMOS circuits for many years has been recognized as an advantageous method to detect defects which are normally missed by conventional logic testing. But one of the main difficulties in this testing is setting the threshold value. A circuit that draws more current than the threshold value of $\text{I}_{\text{DDQ}}$ for any input test vector is declared defective. A circuit that draws less current than the threshold value of $\text{I}_{\text{DDQ}}$ is considered non-defective. If the threshold value is set too high, then circuits that contain defects may be considered non-defective. If the threshold value is set too low, then circuits that are free of defects may fail the $\text{I}_{\text{DDQ}}$ test. On one hand deep-submicron CMOS technologies have allowed increased transistor density chips, on the other hand the leakage current has also increased [3-5]. This background current or leakage current may sometimes exceed the quiescent current in a chip thus making it difficult for the $\text{I}_{\text{DDQ}}$ circuit to detect faulty currents. Process variations of the fabrication of electrical circuits further complicate the determination of the $\text{I}_{\text{DDQ}}$ threshold value [6]. These variations result in differences that exist between individual circuits of the same circuit design. Two integrated circuits of the same design can draw different $\text{I}_{\text{DDQ}}$ values for the same set of input test vectors due to process variations between the two circuits [7]. So, a method of
IDDQ testing which does more than compare measured values of IDDQ against a single threshold was considered for the useful life of IDDQ testing.

Based on the terminology used in [8], one can distinguish between two kinds of current defects: 1) passive defects: involve only nodes of the tested circuit that are not switching, and 2) active defects: involve nodes of the tested circuit that are switching. Examples of passive defects include direct shorts between V_DD and GND and leaky non-switching reversed-biased p-n junctions, such as between the well and substrate. Examples of active defects involve switching nodes of the circuit which include gate oxide shorts, gate drain shorts, drain to GND and drain to V_DD. Figure 1 shows passive and active faults. Figure 1.1(a) shows a minimum size transistor three input defect-free gate. Figure 1.1(b) shows an active defect with a resistive short. This short can conduct IDDQ current or not. It doesn’t conduct current for any test vector resulting in AB=0. It conducts only when AB=1. Finally the same resistive short when connected between V_DD and GND as in Figure 1.1(c) will generate excessive IDDQ current for all test vectors applied to the circuit with this gate. Apart from these there are defects which are caused by open circuits; they break the circuit connections, instead of adding extra ones. Some opens may cause current to flow, however, either because they cause a transistor gate to float in such a way that the transistor is stuck-on, or because they cause an intermediate voltage at a gate input. IDDQ testing tries to detect both kinds of defects (active and passive) by comparing to a single threshold the maximum measurement of quiescent current over a set of test vectors. But this practice is possible only when the average current caused by a defect is significantly higher than the average quiescent current of non faulty ICs, and that there is a small variation of quiescent current over a test sequence and from one chip to another. Actual technology tendencies due to scaling make this
Figure 1.1: Defect-free (a) and defective circuits (b and c).
practice less and less efficient. The two averages just mentioned are becoming closer and closer with technology scaling [9]. So there is definitely need for further research in these testing methods.

These limitations with conventional I_{DDQ} testing has led to the method of I_{DDQ} testing which does more than compare measured values of I_{DDQ} against a single threshold. ∆I_{DDQ} test has been identified as one of the most promising alternatives and possible way to extend the usability of I_{DDQ}. From the ∆I_{DDQ} test techniques which have been implemented so far we can define ∆I_{DDQ} as a test which performs some type of comparison between two or more measurements to decide if the circuit is defective or not. It can be also defined sometimes based on the techniques in which the circuit is able to remember the measurements in a previous time or location. So, ∆I_{DDQ} testing uses some differential measurements instead of measurements based on single threshold as in a conventional I_{DDQ} testing. Based on the ∆I_{DDQ} techniques which have been popular so far this testing is a difference in power supply current between maximum and minimum readings within a testing period [10]. Since the manufacturing process parameters can vary from wafer to wafer, different levels of background current (leakage current) may occur. If process parameters increase the background current, all I_{DDQ} tests will observe a similar increase. Whereas the ∆I_{DDQ}, however, will remain approximately the same and will increase proportionately to the I_{DDQ} readings [11]. Thus, ∆I_{DDQ} is particularly attractive because the differential measurements suppress the influence of the background current.

Though many ∆I_{DDQ} current monitors have been proposed till date none of them have been successfully applied in testing of mixed signal integrated circuits [6,8,10,12-15,16,32]. In this work, a ∆I_{DDQ} built-in current sensor has been presented which provide
digital output for supply current monitoring and testing of a low voltage 12-bit DAC with supply voltage range of 0 to 2.5 V. The built-in current design is based on methods presented in [12, 32] and uses the power supply discharging phenomena. It comprises of a capacitor, switch, comparator and a counter. The 12-bit DAC uses a low voltage op-amp (0 to 2.5 V) and is based on folded cascode configuration. It also uses an additional bulk driving circuitry for the op-amp to operate from 0 to 0.7 V. The DAC chip is designed in 0.5µm n-well CMOS process.

1.1 Literature Review

This following section has a brief review of some of the selected works on ∆I_{DDQ} testing.

- Current Signatures

  A first significant breakthrough for ∆I_{DDQ} testing occurred when the concept of current signatures was proposed [8]. Traditionally, testing of a circuit ends as soon as the circuit fails the I_{DDQ} test. Gattiker and Maly [13] have proposed that I_{DDQ} values be measured for a complete set of input vectors. A complete set of input test vectors include enough test vectors to completely exercise the functionality of the circuitry within the circuit being tested. From the measured values of I_{DDQ}, a “current signature” is generated. The “current signature” includes an ordering of the I_{DDQ} measurements from the smallest value to the largest value. Gattiker and Maly claim that the magnitude of the measurements is not as important as the shape of a plot of the current signature. If there are no large jumps in the plot of the current signature, then the circuit is designated as non-defective. If the plot of the current signature includes any significant jumps or discontinuities, then the circuit is designated as defective. However, in production test, a current signature of the above type cannot be directly implemented in the present-day integrated circuit manufacturing environments. This is because it requires a complete set
of input vectors to be applied to the integrated circuit under test and the resultant measured values of $I_{DDQ}$ for each input vector to be analyzed. Determination of the values of $I_{DDQ}$ for a complete set of input vectors takes too long to implement in a circuit manufacturing environment at a reasonable cost.

Working on the basis of the fundamental property of a current signature being the presence or absence of “steps”, a differential current scheme suitable for production test was proposed again by Gattiker and Maly [13]. A current measurement was based on subsequent vectors producing currents which differed from the first value (either higher or lower) by some threshold.

- **Probabilistic Approach**

  A more recent approach was described by Thibeault [14] in which individual vector differential $I_{DDQ}$ measurements are used. Here, the differences in $I_{DDQ}$ measurements between any vector and its subsequent one are used in a probabilistic manner to determine if a chip is defective or not. In terms of production test, this approach suffers from the requirement to make a large number of absolute measurements of $I_{DDQ}$.

  Both the above approaches are equivalent in rejecting the die, based on some threshold of current differences. As a result they also suffer from the effects of process variation. Ultimately a threshold has to be set in order to determine a PASS/FAIL result.

- **Current Ratio**

  In this method, the ratios of the maximum and minimum $I_{DDQ}$ current are considered. It was observed that the ratio remains relatively constant for the fault free circuits [15]. A leaky chip will leak current proportionally for all vectors and, therefore its current ratios will be similar to that of fault free chip, so the vectors which give maximum and
minimum $I_{DDQ}$ currents should be chosen carefully. One of the main problems facing this method is setting the threshold for the current ratio. If the threshold is too small it will lead to yield loss. This method is not very effective for passive defects because with passive defects the current ratio decreases with increasing background current and it will be difficult to determine the lower threshold for the current ratios.

- **Nearest Current Ratios (NCR)**

  This method is based on the fact that two neighboring dies will have the same $I_{DDQ}$ current for the same vectors. If a ratio of the $I_{DDQ}$ is taken it should be ideally one. The NCR method is self-calibrating because the NCR is ideally equal to one [16]. Due to process variations NCR values vary. NCRs are obtained for all vectors considering all adjacent neighbors. The maximum value of NCR is used for screening defective chips.

1.2 Chapter Organization

In the following chapters, the basis, principles, circuit design, technology considerations, transient simulations, post layout measurements and experimental results are discussed.

**Chapter 2** explains the basic structure and operation of a 12-bit charge scaling digital to analog converter (DAC) and also looks into the in detail analysis of low voltage op-amp used in the DAC. Post layout simulations results of each module of the DAC are included.

**Chapter 3** briefs about the concept of $I_{DDQ}$ testing, and then explains in detail about the design and implementation of a built-in current sensor. The mechanism of fault simulation and fault detection in a 12-bit charge scaling DAC using the BICS is explained along with the post layout simulation results.

**Chapter 4** describes the simulation results and design considerations of a 12-bit charge
scaling DAC and the $\Delta I_{DDQ}$ BICS. Description of the abnormal current behavior and fault
detection in DAC is explained and simulation results are presented. Experimental results
of the fabricated device are presented, compared with SPICE simulations.

Chapter 5 provides a summary of the work presented and scope for future work.

The MOS model parameters used for design is presented in Appendix A. The
entire chip testing procedure is presented in Appendix B.
CHAPTER 2
DIGITAL-TO-ANALOG CONVERTER (DAC) DESIGN

The conversion between analog and digital signals is one of the most important functions in signal processing. The digital-to-analog conversion is a process in which digital words are applied to the input of the DAC as the parallel binary signals which are then converted to an equivalent analog signal by scaling a reference. This analog signal represents the digital word applied. In this conversion process, an N-bit digital word is mapped into a single analog voltage. Typically, the output of the DAC is a voltage that is some fraction of a reference voltage, such that [17, 18]

\[ V_{\text{OUT}} = F \cdot V_{\text{REF}}, \]  

\[ \text{(2.1)} \]

where \( V_{\text{OUT}} \) is the analog voltage output. \( V_{\text{REF}} \) is the reference voltage. \( F \) is the fraction defined by the input word, \( D \), that is \( N \) bits wide. The number of input combinations represented by the input word \( D \) is related to the number of bits in the word by

\[ \text{Number of input combinations} = 2^N. \]  

\[ \text{(2.2)} \]

The maximum analog output voltage for any DAC is limited by the value of some reference voltage \( V_{\text{REF}} \). If the input is an \( N \)-bit word, then the value of the fraction, \( F \), can be determined by,

\[ F = \frac{D}{2^N}. \]  

\[ \text{(2.3)} \]

Figure 2.1 shows a conceptual block diagram of a DAC converter. The inputs are a digital word of \( N \)-bits (\( b_1, b_2, b_3, \ldots, b_N \)) and a reference voltage, \( V_{\text{REF}} \). The voltage output, \( V_{\text{OUT}} \), can be expressed as

\[ V_{\text{OUT}} = K \cdot V_{\text{REF}} \cdot D \]  

\[ \text{(2.4)} \]

Where \( K \) is a scaling factor and the digital word \( D \) is given by
Figure 2.1: Block diagram of a digital-to-analog converter.
\[ D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} + \ldots + \frac{b_N}{2^N} \] (2.5)

N is the total number of bits of the digital word, and \( b_N \) is the \( N^{th} \) coefficient and is either 0 or 1. Thus, the output of a DAC can be expressed by combining Eqs. 2.4 and 2.5 to get

\[ V_{\text{OUT}} = K V_{\text{REF}} \left( \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \frac{b_4}{2^4} + \ldots + \frac{b_N}{2^N} \right) \] (2.6)

The basic architecture of a DAC without a sample and hold circuit at the output is shown in Figure 2.2. The various blocks are a voltage reference, which can be supplied externally, binary switches, a scaling network, and an output amplifier. The voltage reference, binary switches, and scaling network convert the digital word as either a voltage or current signal, and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of conversion.

### 2.1 Performance Specifications of Digital-to-Analog Converter

The following are some of the important static and dynamic performance parameters used to characterize a DAC [17, 18].

- **Least Significant Bit (LSB)**

  LSB refers to the rightmost bit in the digital input word. The LSB defines the smallest possible change in the analog output voltage. The LSB will always be denoted as \( D_0 \). One LSB can be defined as

  \[ 1_{\text{LSB}} = \frac{V_{\text{REF}}}{2^N} \] (2.7)

- **Differential Nonlinearity (DNL)**

  The DNL gives a measure of how well a DAC can generate uniform analog LSB multiples at its output. It is defined as follows

  \[ \text{DNL}_n = \text{(actual increment height of transition, n)} - \text{(ideal increment height)} \]
Figure 2.2: Basic architecture of DAC without the S/H circuit.
where ‘n’ is the number corresponding to the digital input transition. DNL is illustrated in Figure 2.3 for a 3-bit DAC. The change from 101 to 110 results in a maximum +DNL of 1.5LSBs (DNL = 2.5LSB – 1LSB). The maximum negative DNL is found when the digital input code changes from 011 to 100 which is -1.5LSBs (DNL = -0.5LSB – 1LSB). A DAC having greater than $\pm 1/2\text{LSB}$ of DNL actually has a resolution of a DAC, which is less than a bit. That is if a 3-bit DAC has a DNL greater than $\pm 1/2\text{LSB}$ it is considered to be having a resolution of 2-bit DAC. The DNL Characteristics of a 12-Bit DAC is shown in Figure 2.4.

- **Integral Nonlinearity (INL)**

Another important static characteristic of a DAC is called integral nonlinearity (INL). It is defined as the difference between the data converter output values and reference straight line drawn through the first and last output values as shown in Figure 2.3. INL defines the linearity of the overall transfer curve and can be described as follows:

$$\text{INL}_n = (\text{output value for the input code, } n) - (\text{output value of the reference line at the point}).$$

In Figure 2.3 the maximum +INL is 1.5LSB and the maximum –INL is 1.0LSB. Even in this case a DAC should have $\pm 1/2\text{LSB}$ for good resolution. The DNL Characteristics of a 12-bit DAC is shown in Figure 2.5.

- **Offset Error**

Offset error is a constant difference between the actual finite resolution characteristics and the ideal finite resolution characteristic measures at any vertical jump. It is shown in Figure 2.6. The offset error for the 12-Bit DAC is shown in Figure 2.7.
Figure 2.3: Illustration of INL and DNL in a 3-bit DAC.
Figure 2.4: Measured DNL characteristics of a 12-bit DAC.
Figure 2.5: Measured INL characteristics of a 12-bit DAC.
• **Gain Error**

Gain error is the difference between the actual finite resolution and an infinite resolution characteristic measured at the rightmost vertical jump. It is shown in Figure 2.8.

• **Dynamic Range**

Dynamic range is defined as the ratio of the largest analog output value (Full Scale (FS)) to the smallest analog output value. The dynamic range in decibels is given by,

\[ \text{DR} = 20 \log (2^N - 1) \text{ dB.} \]  

(2.8)

For our design, which is a 12-bit, charge-scaling DAC, the dynamic range is 72.24 dB.

• **Resolution**

It is described as the smallest change in the analog output with respect to the value of the reference voltage \( V_{\text{REF}} \). The resolution is given by [17].

\[ \text{Resolution (N)} = \log_2 \left( \frac{V_{\text{REF}}}{1\text{LSB}} \right) = \log_2 \left( \frac{2V}{0.5mV} \right) = 12\text{bits} \]  

(2.9)

### 2.2 Digital-to-Analog Converter Architecture

A wide variety of DAC architectures exist, ranging from very simple to complex. Each of course, has its own merits. There are primarily three architectures of DAC namely-

- Current Scaling
- Voltage Scaling
- Charge Scaling
- **Current Scaling**

The current scaling based DAC architecture is shown in Figure 2.9 [18]. The DAC
Figure 2.6: Illustration of the offset error in a 3-bit DAC.
Figure 2.7: Offset and gain error of a 12-bit DAC.
Figure 2.8: Illustration of gain error in a 3-bit DAC.
architecture uses current through out the conversion known as current steering. This type of DAC requires precision current sources that are summed in various fashions. Since there are no current sources generating \( i_{OUT} \) when all the digital inputs are zero, the MSB, \( D_{2^{n-2}} \), is offset by two index positions instead of one. The binary signal controls whether or not the current sources are connected to either \( i_{OUT} \) or GND. The output current \( i_{OUT} \) has the range of

\[
0 \leq i_{OUT} \leq (2^N - 1)I
\]

where \( I \) is a current source.

One advantage of the current steering DACs is the high-current drive inherent in the system. Of course, the precision needed to generate high resolutions is dependent on how well the current sources can be matched or the degree to which they can be made binary weighted. Another problem associated with this architecture is the error due to the switching.

- Voltage Scaling

In this architecture, the analog output voltage is divided uniformly among the resistor string as shown in Figure 2.10 [18]. Depending on the input digital word, the switches shown close or open if the input is a ‘high’ or ‘low’ voltage, respectively. The analog output is simply the voltage division of the resistors at the selected tap. The value of the voltage at the tap associated with the \( i_0 \) resistor is given by [18],

\[
V_{i, \text{ideal}} = \frac{(i)V_{\text{REF}}}{2^N}, \quad \text{for } i=0, 1, 2, 3...2^N - 1
\]

This architecture typically results in good accuracy, provided that no output current required and that the values of the resistors are within the specified error tolerance of the converter. Another problem with this architecture is the balance between the area
Figure 2.9: Current scaling based DAC architecture.
and power dissipation. So this architecture is not suited for high resolution DACs.

- **Charge Scaling**

A very popular architecture used in the CMOS technology is the charge scaling DAC and is shown in Figure 2.11(a). In this architecture, a parallel array of the binary weighted capacitors, \(2^N C\), is connected to the op-amp, where \(C\) is a unit capacitance of any value. After initially being discharged, the digital signal switches each capacitor to either \(V_{\text{REF}}\) or ground (GND) causing the output voltage, \(V_{\text{OUT}}\), to be a function of the voltage division between the capacitors. Since the capacitor array totals \(2^N C\), if the MSB is ‘high’ and the remaining bits are ‘low’, then a voltage divider occurs between the MSB capacitor and the rest of the array. The analog voltage, \(V_{\text{OUT}}\) from eqs (2.1) and (2.2) becomes

\[
V_{\text{OUT}} = V_{\text{REF}} \cdot \frac{2^{N-1} C}{(2^{N-1} + 2^{N-2} + \ldots + 4 + 2 + 1 + 1)C} = V_{\text{REF}} \cdot \frac{2^{N-1} C}{2^N C} = \frac{V_{\text{REF}}}{2}
\]  

(2.12)

which confirms the fact that the MSB changes the output of a DAC by \(\frac{1}{2} V_{\text{REF}}\). Figure 2.11(b) shows the equivalent circuit under this condition. Therefore, the value of \(V_{\text{OUT}}\) for any digital word is given by [18]

\[
V_{\text{OUT}} = \sum_{K=0}^{N-1} D_K 2^{K-N} V_{\text{REF}} \text{ where } K=0, 1 \ldots N-1.
\]  

(2.13)

The 12-bit DAC used in our design uses charge scaling DAC. The unit capacitance in the DAC is 200fF. The reference voltage used is 2 V, \(V_{\text{SS}}\) is -2.5V and \(V_{\text{DD}}\) is +2.5V.

**2.2.1 Charge Scaling DAC Using Split Array Method**

The charge scaling architecture is very popular among CMOS designers because of its simplicity and relatively good accuracy. However, as the resolution increases, the size of the MSB capacitor becomes a major concern. Split array method reduces the size of the
capacitors [18]. This architecture is slightly different from the charge scaling DAC pictured in Figure 2.11(a). Figure 2.12(a) shows a 5-bit charge scaling DAC using charge scaling method. In this the output is taken off a different node and an additional attenuation capacitor is used to separate the array into a LSB array and a MSB array. The LSB, D₀, corresponds to the leftmost switch and that the MSB, D₅, corresponds to the rightmost switch. The value of the attenuation capacitor is found by

\[ C_{\text{Atten}} = \frac{\text{sum of the LSB array capacitors}}{\text{sum of the MSB array capacitors}} \cdot C, \tag{2.14} \]

where the sum of the MSB array is equal to the sum of the LSB capacitor array minus C. The value of the attenuation capacitor has to be such that the series combination of the attenuation capacitor and the LSB array, assuming all bits are zero, is equal to C. If D₅ is one and the remaining bits are all zero, then the equivalent circuit for the DAC can be represented by Figure 2.12(b). The expression for the output voltage then becomes

\[ V_{\text{OUT}} = \frac{4}{8 \cdot \frac{7}{8}} \cdot V_{\text{REF}} = \frac{1}{2} V_{\text{REF}} \tag{2.15} \]

which is the same result as that of eq 2.12 of the simple charge scaling DAC of Figure 2.11(a). So in this way the split array method is as compatible as the regular charge scaling DAC. Added to that it as the resolution increases this method will reduce the size of the capacitance required to a far greater extent.

### 2.3 Digital-to-Analog Converter (DAC) Operation

The presented DAC design uses the charge scaling method [17, 18] and operates in low voltage with supply range from 0 to 2.5 V. The basic circuit diagram of a 12-bit charge scaling DAC using split array method is shown in the Figure 2.13. This circuit converts
Figure 2.10: Resistor string DAC.
Figure 2.11: (a) Charge scaling DAC architecture.

Figure 2.11: (b) Equivalent circuit with MSB=1 and all other bits set to zero.
Figure 2.12: (a) 5-bit charge using scaling DAC using split array method.

Figure 2.12: (b) Equivalent circuit with MSB=1 and all other bits set to zero.
the 12-bit digital input word to a respective analog signal by scaling a reference that is obtained by the capacitive network. Figure 2.13 shows the various blocks associated with the DAC which constitute the operational amplifier, sample-and-hold circuit (S/H), capacitive network and the multiplexer switches to which the digital word is given. Initially the input digital word is given to a multiplexer circuitry. Depending on the logic value of each bit of the word, the multiplexer chooses the particular voltage to which the capacitor is to be charged. If the input bit in the digital word is logic ‘0’ then the multiplexer chooses input which is connected to the ‘GND’ and the capacitor is charged to ‘GND’ and if the input bit in the digital word is logic ‘1’ then the capacitor is charged to $V_{\text{REF}}$. The capacitor at the end of the network is used as a ‘terminating capacitor’. Depending on the capacitors, which are charged to different voltages based on the input digital word, the effective resultant analog voltage is calculated for the respective digital combination. The analog voltage is passed through the op-amp and through the sample-and-hold circuit and appears as analog voltage. Thus, the digital-to-analog conversion is performed. Different blocks of the DAC are discussed in the following sections.

2.3.1 Capacitor Array Design

The architecture of DAC’s capacitive array is drawn using a unit capacitor of 200 fF with two poly silicon layers poly1 and poly2. Figure 2.14 shows the layout of the unit capacitor used in the design. This unit capacitor configuration reduces the effect of various errors introduced during fabrication. In the fabrication process of on-chip capacitors, the capacitance values of a single capacitor up to 10 to 30 vary with percent from the desired value. Because of this, it is difficult to produce high accuracy capacitors in a standard CMOS process as well as integrated circuits, which rely on the accuracy of a single capacitance value. If, instead, capacitance ratios are used, the relative error is
Figure 2.13: Schematic block diagram of 12-bit charge scaling DAC with $V_{DD} = 2.5V$, $V_{SS} = 0V$ and $V_{GND}$
cancelled since it is the ratio of the capacitance that is taken into consideration but not the single capacitance value alone. Figure 2.15 shows the layout of the capacitor array using unit capacitor configuration. The array is surrounded with dummy capacitors and guarded by the guard ring to cancel out the effect of parasitics.

The capacitors, which are present at the end of the arrays, do not have the surrounding capacitors to cancel out the relative error. To take care of these capacitors dummy capacitors are added to the array [19]. Figure 2.16 shows the use of dummy capacitors in the capacitor array layout. The substrate noise present in the substrate can be coupled to the capacitor through its parasitic capacitor and any voltage variation present is also coupled to other components of the chip. To avoid this coupling capacitor, array is shielded from the substrate with N-well under it and connecting it to a quiet DC potential [19]. The guard rings are used in the layout around the capacitor array to prevent from any sort of interference.

2.3.2 Operational Amplifier (Op-Amp) Summary

The operational amplifier designed for the 12-bit DAC is a low voltage op-amp with supply voltage range of 0 to 2.5 V. Before going to actual design, a brief summary about the motivation and implications of low power design is discussed. As CMOS technology continues to shrink in size, there are several important implications that result. The motivation for decreasing the channel length (which results in shrinking of size) [20] is to increase the cut-off frequency $f_T$ of the MOSFET and to allow more circuits to be implemented in the same physical area, which sustains the move from very large-scale integrated (VLSI) circuits to ultra large-scale integrated (ULSI) circuits. The reduction in voltage is due to scaling down of the technology. In addition, the power dissipation in ULSI circuits, it is necessary to either cool the chip to reduce the power supply or both.
Figure 2.14: Layout of a parallel plate capacitor (C=200 fF).
Figure 2.15: Layout of the capacitor array using unit capacitor configuration.
Figure 2.16: Layout showing dummy capacitors to match the capacitors present at the corner of the capacitor array.
Coming to the implications that result from low power, we have firstly decreased dynamic range. Apart from the higher limit of the dynamic range which can be reduced by differential operation there is also lower limit which is of main concern. Secondly and probably one of the biggest concerns with reduced power supplies is the input common-mode voltage range (ICMR) over which the differential input works as desired. Even if the ICMR is sufficiently large, it necessary that it be centered within the power supply range. The ICMR is important because it determines if the output of a stage can interface with the input of another different or similar stage. Another important implication is larger capacitance, for low power, lower $V_{DS}$ (sat) are required and this is obtained by large values of $W/L$ which further leads to larger capacitances. All the above implications are taken care of in the present design of the op-amp whose block diagram is shown in Figure 2.17. In Figure 2.17 the differential stage consisting of NMOSFETS operate in both saturation and bulk driven modes which results in good ICMR. The design also has lower $W/L$ MOSFETS to reduce large capacitances and also has extra high swing cascode current source apart from a class A amplifier to increase the output swing (dynamic range).

- **Bulk Driven MOSFET**

With bulk-driven mode MOSFETS, it is possible to get reasonable values of ICMR with the power supply voltages down to 1V. Figure 2.18 [17] shows the cross section of an n-channel bulk-driven MOSFET. The current control mechanism forms the depletion region formed between the well and the channel. As the depletion region widens, it pinches off the channel. This depletion characteristic allows the ICMR to extend below the negative power supply for an n-channel input. The bulk-driven operation requires that the channel be formed, which is accomplished by a fixed bias applied to the gate terminal.
Figure 2.17. Schematic diagram of the designed operational amplifier showing different divisions. Note: For the P-MOSFETS the substrate is connected to $V_{DD}$. 
of the MOSFET. When a negative potential is applied to the bulk with respect to the source, the channel-bulk depletion region becomes reverse biased and widens. If the negative bulk voltage is large enough, the channel will pinch off. Figure 2.19 [17] shows the drain current of the same n-channel MOSFET when the bulk-source voltage is varied and when gate-source voltage is varied. The large signal equation for the bulk driven MOSFET is given by,

$$i_D = \frac{K_n}{2L} \left[ V_{GS} - V_{T0} - \gamma \sqrt{2|\phi_F| - V_{BS}} + \gamma \sqrt{2|\phi_F|} \right],$$  \hspace{1cm} (2.16)

where the small signal transconductance is,

$$g_{mbs} = \frac{\gamma \sqrt{(2k_nW/L)I_D}}{2 \sqrt{2|\phi_F| - V_{BS}}}.$$  \hspace{1cm} (2.17)

The small signal channel conductance does not change for bulk-driving. Normally, $V_{BS}$ is negative but sometimes it is useful to operate the bulk-driven MOSFET with bulk-source junction slightly forward biased. One advantage is that transconductance given by Eq. (2.17) would increase and could become larger than the top gate transconductance.

The bulk-source driven transistor can be used as the source-coupled pair in a differential amplifier as shown in Figure 2.20 [17]. The depletion characteristics of the bulk-source-driven transistors will allow the ICMR to extend below the negative power supply for an n-channel input. As the common mode voltage of Figure 2.20 begins to increase the small signal transconductance increases. This can be seen as follows. First we note that if the current through M1 and M2 is constant due to M5, then $V_{BS}$ must be constant. Therefore, if $V_{icm}$ increases, the sources of M1 and M2 increase. However, if sources of M1 and M2 increase, then $V_{GS}$ decreases and the current would not remain
constant. In order to maintain the currents in M1 and M2 constant, the bulk-source junction becomes less reverse biased, causing the effective threshold voltage to decrease. If $V_{icm}$ is increased more, the bulk-source junctions of M1 and M2 will become more forward biased and input current will start to flow. As a consequence of these changes in $V_{BS}$, the transconductance is given by Eq. (2.17) increases because $V_{BS}$ is becoming less negative and then becoming positive.

### 2.3.3 Low-Voltage Two Stage Op-amp Topology

The op-amp designed is based on the low voltage op amp of [17] but with bulk driven n-MOSFETS for the input differential stage and also some additional circuitry for improving the output swing. Figure 2.21 shows the schematic of the actual design which shows various stages. Before the actual analysis is done a brief review of the circuit is presented. The input stage constituting of M1-M2 is the simple n-channel differential amplifier with current source loads M3-M4. This gives the widest possible input common-mode range for the differential pair. The signal currents of the differential output are folded through the transistors M6 and M7 and converted to single-ended signals with the n-channel current mirror constituting M8 and M9. Transistors M15, Mb and M16 constitute the biasing circuitry. Also there is an additional biasing circuitry M21- M23. The transistors M17-M20 constitute the bulk driving circuitry for the differential pair enabling the n-channel transistors of differential pair to respond to input voltages below 0.7 V. Also there is a high swing circuitry constituting M10-M12 which is responsible for high output swings and finally there is a second stage Class-A amplifier.

---

Figure 2.18: Cross section of an n-channel bulk-driven MOSFET.
Figure 2.19: Transconductance characteristics of the MOSFET of Figure 2.18 for bulk-source-driven and gate-source-driven modes of operation.
Figure 2.20: Low voltage differential input using bulk-source-driven input transistors.

### 2.3.4 Operational Amplifier Design

- **Input Stage and the Biasing Circuitry**

As shown in Figure 2.21, input stage of the operational amplifier consists of two transistors M1-M2 which constitute a simple n-channel differential amplifier with two more transistors M3-M4 as current source loads. This gives the widest possible input common mode range for the differential pair. Coming to the biasing circuitry, as shown in Figure 2.21, M15 and M3 and also M15 and M4 act as p-MOS current mirrors serving as current source, M16 and M5 act as n-MOS current mirror serving as current sink as shown in Figure 2.21. Coming to the design of these transistors, initially a bias current of 20 µA is assumed. Figure 2.22 and Figure 2.23 show PMOS and NMOS current mirrors respectively which are extracted from the actual design of Figure 2.21. From Figure 2.23 we see that both the transistors have same gate to source voltage, and are in saturation region of operation. The current is given by the following equation.

For n-MOS current mirror, we can write,

\[
\frac{I_{\text{out}}}{I_{\text{Ref}}} = \left( \frac{W_5}{L_5} \right) / \left( \frac{W_{16}}{L_{16}} \right).
\]  

(2.18)

For \( \left( \frac{W_5}{L_5} \right) / \left( \frac{W_{16}}{L_{16}} \right) = 1 \),

\[
I_{\text{OUT}} = 1 \ast I_{\text{REF}} = 20 \mu A
\]  

(2.19)

Thus, the current through \( I_5 = 20 \mu A \)

For identical size transistors, the ratio is unity, which means the output mirrors the input current, which is what is shown above.

Also from Figure 2.21, \( W_{15}/L_{15} = W_{16}/L_{16} \) as the same bias current flows in both of them.

Therefore now \( W_{15}/L_{15} = W_{16}/L_{16} = W_5/L_5 \)  

(2.20)
Figure 2.21: Schematic diagram of the operational amplifier showing W/L ratios of all the transistors.

Note: For the P-MOSFETS the substrate is connected to $V_{DD}$. 

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (µm/µm)</th>
<th>Transistor</th>
<th>W/L (µm/µm)</th>
<th>Transistor</th>
<th>W/L (µm/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>3/1.2</td>
<td>M10</td>
<td>6/0.6</td>
<td>M17</td>
<td>3/0.6</td>
</tr>
<tr>
<td>M2</td>
<td>3/1.2</td>
<td>MR</td>
<td>0.9/1.8</td>
<td>M18</td>
<td>2.7/6</td>
</tr>
<tr>
<td>M3</td>
<td>9/0.6</td>
<td>M11</td>
<td>3/6</td>
<td>M19</td>
<td>3.3/1.8</td>
</tr>
<tr>
<td>M4</td>
<td>9/0.6</td>
<td>M12</td>
<td>0.9/0.9</td>
<td>M20</td>
<td>5.7/3</td>
</tr>
<tr>
<td>M5</td>
<td>6/0.6</td>
<td>M13</td>
<td>2.7/5.1</td>
<td>M21</td>
<td>3/0.6</td>
</tr>
<tr>
<td>M6</td>
<td>3.3/0.6</td>
<td>M14</td>
<td>0.9/0.9</td>
<td>M22</td>
<td>1.8/2.4</td>
</tr>
<tr>
<td>M7</td>
<td>3.3/0.6</td>
<td>M15</td>
<td>6/0.6</td>
<td>M23</td>
<td>2.1/2.1</td>
</tr>
<tr>
<td>M8</td>
<td>3/0.9</td>
<td>M5</td>
<td>3/1.5</td>
<td>Cc</td>
<td>316fF</td>
</tr>
<tr>
<td>M9</td>
<td>3/0.9</td>
<td>M16</td>
<td>6/0.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Knowing that the current through M5 is 20 μA we conclude that the current through M1 and M2 are 10 μA as M1 = M2.

**Double to Single Ended Conversion Stage**

The signal currents of the differential output are folded through the transistors M6 and M7 and converted to single-ended signals with the n-channel current mirror (M8 and M9). As the source-gate voltages and currents M6 and M7 are same we can say that same amount of current flows through both of them. As such their sizes are equal, \( \frac{W_6}{L_6} = \frac{W_7}{L_7} \), and so if we assume a current of 20 μA through both of them then 30 μA flows through M3 and M4. M8 and M9 act as a current mirror to convert signal currents from M6 and M7 to single-ended signal and the sizes of both are equal as same current passes through both of them.

**High Swing Circuitry**

In Figure 2.21, M12, M11, MR and M10 constitute the high swing cascode current source for the op-amp. We see from the Figure 2.21 that the ON voltage (saturation voltage or \( V_{GS-V_T} \)) of M4 is \( V_{ON} \), this gives the source-gate voltage of M6 and M7 as \( V_T + V_{ON} \), which in turn makes the voltage across M12 as \( V_T + 2V_{ON} \). So this is the minimum drain voltage required for M11 to allow a large range of \( V_{OUT} \) values. To explain the phenomena of high swing cascode current source more clearly, consider the self-biased high swing cascode current source circuitry shown in Figure 2.24. Our main purpose is to avoid the dependence of voltage swing on \( V_T \), because although \( V_{ON} \) can be controlled by changing the W/L ratios, the threshold term \( V_T \) cannot be controlled and represents a significant loss of voltage swing when current mirror is used as an active load in an amplifier. In order to achieve this, design of the circuit is in such a way that the drain voltage of M2 is as minimum as possible and defines this voltage as \( V_{MIN} \). We
Figure 2.22: PMOS current mirror design.
Note: For the P-MOSFETS the substrate is connected to $V_{DD}$.

Figure 2.23: NMOS current mirror design.
Note: For the P-MOSFETS the substrate is connected to $V_{DD}$. 
know that for M2 to be in saturation,

\[ V_{D2} \geq V_{G2} - V_T \]  

(2.21)

Since \( V_{G2} = V_T + 2V_{ON} \), substituting this value into above equation gives

\[ V_{D2} \text{ (min)} = V_{MIN} = V_T = 2V_{ON}. \]  

(2.22)

The current voltage characteristics of Figure 2.24 are illustrated in Figure 2.25 where the value of the \( V_{MIN} \) of Eq. (2.22) is shown. \( V_{MIN} \) is dropped across both M1 and M2, which is \( V_{ON} \) on each of the transistors. Also from Figure 2.24 \( V_{DS} \) of M1 is equal to \( V_{DS} \) of M3, so \( i_{OUT} \) will be an exact replica of \( i_{REF} \).

- **Bulk Driving Circuitry**

Transistors M17, M19, M18, and M20 constitute the bulk driving circuitry as shown in Figure 2.21. This circuitry acts to enable the n-channel transistors of the differential pair to respond to voltages below 0.7 V. As long as the input to the differential pair is above 0.7 V, the bulk driving circuitry doesn’t supply any voltage to the bulk of M1 and M2 and anyhow the transistors function properly as they operate above their threshold voltages, \( V_T \). When the input voltages go below 0.7 V then bulk driving circuitry comes into picture. When the voltage is 0.7 V, M17 is off and M19 is on and further this turns off M20. Now as M19 is on and there is voltage drop across M19 which appears on the bulk of the input differential pair. This voltage at the bulk of transistors M1 and M2 enables them to respond to input voltages less than 0.7 V.

- **Second Stage or Output Amplifier (Class A amplifier)**

Transistors M14 and M13 constitute the second stage of the op-amp. The purpose of this is to reduce the output resistance and increase the current driving capability. This can be achieved by simply increasing the bias current in this stage. There are several ways to specify the performance of the output amplifier. One way is to specify the output
Figure 2.24: Self-biased high swing cascode current source circuitry. Note: For the P-MOSFETS the substrate is connected to $V_{DD}$.

Figure 2.25: Current voltage characteristics of Figure 2.24.
swing. From Figure 2.26 which is widely used Class-A amplifier as output stage also used in the present design. The maximum sinking current of the output stage of Figure 2.26 is given as

\[ I_{\text{OUT}}^– = \frac{K'_1 W_1}{2L_1} (V_{\text{DD}} - V_{\text{SS}} - V_{T1})^2 - I_Q \]  

(2.23)

where it has been assumed that \( V_{\text{IN}} \) can be taken to \( V_{\text{DD}} \). The maximum sourcing current of the simple output stage of Figure 2.25 is given by

\[ I_{\text{OUT}}^+ = \frac{K'_2 W_2}{2L_2} (V_{\text{DD}} - V_{\text{GG2}} - |V_{T1}|)^2 \leq I_Q, \]  

(2.24)

where \( I_Q \) is the dc current provided by the current source, MP. It can be seen from above equations that the maximum sourcing current will typically be the limit of the output current. Generally \( I_{\text{OUT}}^– > I_{\text{OUT}}^+ \) because \( V_{\text{IN}} \) can be taken to \( V_{\text{DD}} \) strongly turning MN and \( I_Q \) is a fixed current that is normally a constant. Table 2.1 summarizes the W/L ratios of the op-amp.

The amplifier physical layout is made using L-Edit 10.20 and the SPICE simulations of the layout are extracted including the parasitic capacitances. Figure 2.27 shows the transient analysis of operational amplifier. When an input voltage of 900 \( \mu \text{V} \) ac sine wave at a frequency of 50 kHz is applied, we get 2.5 V peak-to-peak output voltage giving a gain of 2800. Figure shows the transfer characteristics obtained from DC sweep analysis. Figure 2.29 shows the frequency response characteristics of the amplifier. The 3 dB gain of the amplifier is approximately 30. Figure 2.30 shows the phase margin which is shown to be 88°.

2.3.5 Unity Follower

A unity follower is basically an amplifier with a gain of unity. It is used mainly as
Figure 2.26: Simple class A amplifier.
a buffer amplifier in order to increase the current driving capability of the amplifier stage.

An ideal unity follower would exhibit infinite input impedance, zero output impedance, large bandwidth and unity gain. The gain-bandwidth product of the amplifier is known, as its figure-of-merit, and is a constant for any given amplifier. It is usually determined for an op-amp by putting it in the unity follower configuration. From basic op-amp theory, we know that the gain of an op-amp in its non-inverting configuration as shown in Figure 2.31 given by

$$V_o = (1 + \frac{R_f}{R})V_i$$  \hspace{1cm} (2.25)

$R_f$ and $R$ are the feedback and series resistances of the op-amp and $V_i$ and $V_o$ are the input and output voltages of the op-amp. The gain of the op-amp is determined by the resistive network alone and is given by,

$$A_v = (1 + \frac{R_f}{R})$$  \hspace{1cm} (2.26)

If $R_f$ is zero, then the gain of the amplifier is unity. The input to be buffered is applied to the non-inverting terminal of the unity follower, and the output connected to the inverting terminal of the op-amp in the feedback configuration. So, as the signal increases in strength at the non-inverting terminal, the signal at the inverting end increases too thus forcing the output to follow the input. Only the differential stage of the amplifier discussed was used to realize the unity follower buffer as shown in Figure 2.32. The drain of transistor M13 is coupled back to the gate of the input transistor M1. This connection introduces feedback to the inverting terminal of the op-amp, thus, putting it in the unity follower configuration.
Table 2.1. W/L ratios of transistors in CMOS operational amplifier circuit of Figure 2.21.

<table>
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<td>M12</td>
<td>0.9/0.9</td>
<td>M20</td>
<td>5.7/3</td>
</tr>
<tr>
<td>M5</td>
<td>6/0.6</td>
<td>M13</td>
<td>2.7/5.1</td>
<td>M21</td>
<td>3/0.6</td>
</tr>
<tr>
<td>M6</td>
<td>3.3/0.6</td>
<td>M14</td>
<td>0.9/0.9</td>
<td>M22</td>
<td>1.8/2.4</td>
</tr>
<tr>
<td>M7</td>
<td>3.3/0.6</td>
<td>M15</td>
<td>6/0.6</td>
<td>M23</td>
<td>2.1/2.1</td>
</tr>
<tr>
<td>M8</td>
<td>3/0.9</td>
<td>Mb</td>
<td>3/1.5</td>
<td>C_C</td>
<td>516fF</td>
</tr>
<tr>
<td>M9</td>
<td>3/0.9</td>
<td>M16</td>
<td>6/0.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 2.27: Input and output responses of the operational amplifier.
Figure 2.28: Transfer characteristics of the amplifier.
Figure 2.29: Frequency response characteristics of the operational amplifier.
Figure 2.30: Phase response characteristic of the amplifier, the phase margin is $89^\circ$. 
2.3.6 Sample-and-Hold circuit

The sample-and-hold (S/H) circuit as it is applied is used to maintain a constant output of the DAC during conversion. The S/H circuit used here is with an amplifier with feedback. The use of feedback enhances the accuracy of the S/H. In general, the minimum requirement for S/H is a switch, a storage element and an op-amp with or without feedback [17]. The transmission gate is used as switch, a capacitor as storage element, and a unity-gain op-amp is used for an op-amp with feedback. Figure 2.33 is a block schematic of the sample-and-hold circuit. There are two modes of operation for the circuit: ‘sample’ mode and ‘hold’ mode. In the ‘sample’ mode, the output follows the input, usually with a gain of unity. In the circuit, this sample mode occurs when the transmission gate is on (i.e. when the switch is closed) and the analog signal is sampled on the storage capacitor $C_H$. When the transmission gate switches to ‘hold’ mode (i.e. when the switch is open), $C_H$ is disconnected from its charging source and the output of S/H ideally retains the last value it had when the command to hold was given, and it continues to retain that value until the mode input switches back to ‘sample’. The unity-gain op-amp is used to buffer the voltage across the storage capacitor and also to avoid the large overshoot, which might occur, on the output when the input changes quickly.

- Transmission Gate Switch

Transmission gate is used as input switch to the S/H circuit and is operated by an external control signal to perform the two modes of operation the ‘sample’ and ‘hold’. The external control as shown in Figure 2.33 is $V_{CONROL}$. The switch should ideally offer zero resistance to the signal when it is closed (‘sample’ mode) and infinite resistance when open (‘hold’ mode). So a CMOS transmission gate switch (TG-switch) is constructed by paralleling an n-MOS transistor with a p-MOS transistor. The
Figure 2.31: Non-inverting operational amplifier.
Figure 2. 32: CMOS operational amplifier as a unit gain amplifier. 
Note: For the P-MOSFETS the substrate is connected to $V_{DD}$. 
transmission gate switch can be made to turn ON or OFF for either polarity of the mode control signal by connecting a simple inverter between the gates of the transistor. Since the TG switch has both an n-type and p-type devices, connected in parallel, there is no degradation of the signal whether it is large or small.

- **The Storage Capacitor**

  The storage capacitor limits the slew rate in the *sample* mode and determines the ‘droop’ in the *hold* mode of operation. The slew rate is the rate at which the voltage across the capacitor can change with respect to time and is entirely a function of the input signal frequency. The equivalent circuit of the S/H amplifier during *sample* is that of a low-pass filter with the series resistance of the filter consisting of the TG-switch resistance when closed, and the storage capacitor $C_H$. For the voltage of the capacitor to follow the input signal fairly well, the RC time constant of the filter should be close to the time period of the input signal. The value of the storage capacitor to be used is therefore a function of the input signal frequency. The other consideration for the value of the storage capacitor is the droop rate. ‘Droop’ is the gradual drop in the ‘held’ voltage by the capacitor with time, during the *hold* period. Obviously, this introduces errors in the digital-to-analog conversion process, as the voltage level at any time after the instant it was sampled would be different from the level at which it was sampled. The storage capacitor $C_H$ (6pF) is implemented using the ploy1 and poly2 layers CMOS process. The layout of sample and hold circuit is shown in Figure 2.34 and SPICE simulations of the layout are shown in Figure 2.35.
Figure 2.33: Schematic diagram of sample and hold diagram.
Figure 2.34: Layout of sample and hold circuit. $C_H = 6\text{pF}$
2.4 12-Bit Digital-to-Analog Converter (DAC)

The 12-bit charge scaling DAC is tested by giving various combinations of digital input words and the respective analog output voltage is obtained. The reference voltage used in the design is 2.0 V. The 12-bit charge scaling DAC has about 4096 digital word combinations and is quantized within the reference voltage of 2.0 V with a step of 0.5 mV.

This is obtained as follows:

Total number of input combinations = 4096 (since it is $2^{12}$ combinations of input).

The reference voltage used is 2 V. The least significant change in the output value is

$$\text{LSB} = \frac{2}{4096} = 0.5 \text{ mV}.$$ 

Figure 2.36 shows the layout of the 12-bit DAC. Figure 2.37 shows the DAC output characteristics, for all combinations of the digital input word starting from ‘000000000000’ to all ‘111111111111’s.
Figure 2.35: Post layout SPICE simulations of sample and hold circuit of Figure 2.34.
Figure 2.36: Layout of 12-bit DAC.
Figure 2.37: DAC output characteristics.
CHAPTER 3

ΔI_{DDQ} BUILT-IN CURRENT SENSOR BICS DESIGN

This chapter deals with the basics and the design part of the ΔI_{DDQ} built-in current sensor and implementation of this BICS in a 12-bit charge scaling DAC, the fault simulation and detection methodology. Simulations and layouts of the circuits are also discussed. Apart from these, the chapter also deals with I_{DDQ} testing and its limitations, different types of faults that are found in the circuits.

3.1 I_{DDQ} Testing and Its Limitations in CMOS Integrated Circuits

I_{DDQ} testing is used to detect any defective or faulty current in a circuit. I_{DDQ} testing is also known as quiescent power supply current monitoring. If we can define two states of operation of a circuit i.e., transition state (when there is input transition) and quiescent state (when there is steady state), I_{DDQ} can be defined as the current in a CMOS integrated circuit when all logic levels are in quiescent state. I_{DDQ} testing of CMOS ICs has proved to be very efficient for improving test quality. The test methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects such as the gate oxide shorts, floating gates and bridging faults, which are not very well modeled by the classic fault models, or undetectable by conventional logic tests [21]. In addition, I_{DDQ} testing can be used as a reliability predictor due to its ability to detect defects that do not yet involve faulty circuit behavior, but could be transformed into functional failures at an early stage of circuit life. Figure 3.1 shows a block diagram of I_{DDQ} testing with BICS [21]. Normally this BICS works in two modes, the normal mode and test mode. In the normal mode the BICS is totally isolated from the circuit under test. In the testing mode, it detects the abnormal current caused by
Figure 3.1: Block diagram of $I_{DDQ}$ testing.
permanent manufacturing defects. For defect free situation the magnitude of $I_{DDQ}$ is 10’s of nAs while transient current may reach 10’s of mAs. The BICS is inserted in series with the power supply or GND of CUT to detect abnormal $I_{DDQ}$ current. This BICS checks whether quiescent current is below or above a particular reference current and indicates existence of defects.

Here’s a demonstration of the BICS for $I_{DDQ}$ testing [22] shown in Figure 3.2. In the normal mode it is totally isolated from the CUT, so that the operation of CUT is not affected by it. In the test mode, the BICS compares the quiescent state current with reference current. If the quiescent current is greater than the reference current, the output signal PASS/FAIL is set to ‘1’ or ‘0’ otherwise, wherein ‘1’ implies the existence of defect while ‘0’ reflects no defect. The operation of the BICS shown in Figure 3.2 can be understood with the timing diagram shown in Figure 3.3. In the normal mode, the EXT pin is connected to GND so that the CUT is isolated from the BICS and is floating in the testing mode. In the testing mode, when an input transition occurs, a peak $I_{DD}$ current flows between the power supply and ground. Since this current is inevitable BICS must ignore this current during the transition state. To prevent BICS from detecting this peak current, TCLK is connected to the gate of NMOS transistor Q0 and is connected to $V_{DD}$ in this transition state so that current mirror Q1 and Q2 has no affect and the output PASS/FAIL is not affected. Which means it doesn’t detect the peak current. In the quiescent state, the TCLK is given to GND, therefore Q0 is off and the current mirror replicates the defective current at the output stage. The PMOS current mirror pairs, Q3 and Q4, replicate the constant reference current at the output stage. So, if the $I_{DEF}$ current is greater than $I_{REF}$ current by certain value, the threshold of the final inverter is set in such a way that the output of PASS/FAIL is ‘1’ indicating a defective current.
Figure 3.2. \( I_{DDQ} \) BICS design.
Figure 3.3: Timing diagram showing different stages of operation of CUT.
This process of testing has been effective for quite some years, but as the technology advanced, device size reduced the leakage currents started to increase in comparison to the quiescent currents. So in this case ‘I_{DEF}’ currents in the Figure 3.2 are a mix of both leakage and quiescent currents and still there is every possibility that this current may be equal to the ‘I_{REF}’ current. However these leakage currents are not due to faults, like threshold voltage, leakage current is also affected by the process variations [23].

3.2 Physical Faults in CMOS Integrated Circuits

In CMOS technology, the most commonly observed physical failures are bridges, opens, stuck-at-faults and gate oxide shorts (GOS). These defects create indeterminate logic levels at the defect site [21]. Processing defects cause shorts or break in one or more of the different conductive levels of the device [24]. We briefly discuss these physical defects that cause an increase in the quiescent current.

3.2.1 Open Faults

Figure 3.4 shows a 2-input NAND open circuit defect. Logic gate inputs that are unconnected or floating inputs are usually in high impedance or floating node-state and may cause elevated IDDQ [25]. In Figure 3.4, node V_N is in the floating node-state. For an open defect, a floating gate may assume a voltage because of parasitic capacitances and cause the transistor to be partially conducting [26]. Hence, a single floating gate may not cause a logical malfunction. It may cause only additional circuit delay and abnormal bus current [25]. In Figure 3.4, when the node voltage (V_N) reaches a steady state value, then the output voltage correspondingly exhibits a logically stuck behavior and this output value can be a weak or a strong logic voltage. Open faults, however, may cause only a
Figure 3.4: Open circuit defect.
Note: $V_N$ is an open node as it is floating.
small rise in $I_{DDQ}$ current, which the off-chip current sensor may not detect because of its low-resolution [21]. It can be detected using a BICS. An open source or open drain terminal in a transistor may also cause additional power-bus current for certain input states. In this scope of work, we deal with bridging faults.

### 3.2.2 Bridging Faults

The short circuit faults in very large-scale integrated circuits are popularly termed as bridging faults. With $I_{DDQ}$ measurement, a bridging fault can be detected between two nodes having opposite logical values in the fault-free circuit [26]. Bridging faults can appear either at the logical output of a gate or at the transistor nodes internal to a gate. Inter-gate bridges between the outputs of independent logic gates can also occur. Bridging fault could be between the following nodes: 1) drain and source, 2) drain and gate, 3) source and gate, and 4) bulk and gate. Examples of bridging fault are shown in Figs. 3.5 and 3.6, respectively. Figure 3.5 shows example of possible drain to source bridging faults in an inverter chain in the form of low resistance bridges ($R_1$, $R_2$ and $R_4$). Resistance bridge, $R_3$ is an example of inter-gate bridge. Figure 3.6 shows examples of gate to source and gate to drain bridges in an NAND gate circuit. Bridging faults can be modeled between adjacent metal lines in a 12-bit charge scaling DAC at different conducting levels. We have introduced faults in the 12-bit charge scaling DAC by using “fault-injection transistors” instead of hard metal shorts invented in our group [27]. The introduction of a fault via the “fault-injection” transistor enables the 12-bit DAC to function fault-free under the normal conditions. The faults considered include source-drain bridge, drain-gate bridge and source-gate bridge. Bridging faults cannot be detected in normal logic testing methods, however, can be detected by the $I_{DDQ}$ testing method.
Figure 3.5: Drain source and inter-gate bridging faults in an inverter.
Figure 3.6: Drain-gate and gate-source bridging faults in an inverter.
3.2.3 Gate Oxide Short Defects

Gate-oxide short (GOS) defects occur frequently in CMOS technology. The principle physical reasons for GOS are the breakdown of the gate oxide and the manufacturing spot defects in lithography and processes on the active area and polysilicon masks [28]. Figure 3.7 illustrates the circuit level gate oxide short defect model [26]. These defects can be seen as short-circuits between the gate electrode and the conducting channel of the device through SiO₂. GOS short causes an undesirable current injection into the channel [24, 28]. This current injection results in a substantial increase in the quiescent current. The diode-resistor combination could be used to model the rectifying behavior of the new current path introduced by the defect [28]. These defects are unlikely to produce logical errors, but cause important deviation of parametric specifications especially of the circuit [29].

3.3 $\Delta I_{DDQ}$ BICS Design

$I_{DDQ}$ testing is an important ingredient of the test suite for CMOS ICs. The merits of $I_{DDQ}$ testing in quality improvement, test cost reduction and burn-in elimination have been well recognized [30]. However, the conventional $I_{DDQ}$ testing is not very effective in devices fabricated in deep sub-micron CMOS technology due to the increased sub-threshold current in MOS transistors [3, 31]. Williams et al. [9] in their work presented an expected problem with $I_{DDQ}$ tests as component densities increase and larger blocks of logic are placed on the chip. With denser geometries and higher drive transistors, any additional current ($I_{DDQ}$ Current) caused by potential defects can be less significant in comparison to the background current (leakage current) of the chip. So a conventional $I_{DDQ}$ testing circuit with a reference threshold for which only currents above that
Figure 3.7: (a) Gate-oxide short in a MOSFET and (b) equivalent circuit model. $R_s$ is the effective resistance of the short. The diode (B) models the rectifying behavior of the new current path introduced by the defect.
threshold value are identified as defective currents doesn’t work in this case.

The design that we are going to be discussing is based on the power discharge phenomenon [12, 32]. It includes an on-chip switch connected between the VDD pin and the CUT. As this switch is integrated in the circuit, a faster sensor operation is possible because of the reduction of the circuit’s loading capacitance of the circuit. Figure 3.8 shows a version of Keating–Mayer approach [12]. During the first part of the period, while switching transients in the CUT are drawing large currents, FET (field effect transistor) Q1 provides a short circuit (100 mΩ) between C1 and C2. This maintains full voltage to the CUT. After the transient has settled, Q1 is turned off, so that the static current for the CUT must be supplied by C1. Since the current in CUT is provided by C1, the total charge provided to the CUT, and therefore the current, can be determined from the following equation:

\[
CV = Q = I \times t \tag{3.1}
\]

Or

\[
I = \frac{CV}{t} \tag{3.2}
\]

In order to measure I_DDOQ, simply wait for an appropriate amount of time (few nano sec) and measure the voltage drop across the FET Q1 with a difference circuit as shown in Figure 3.8. The amount of time is not critical; it must be long enough so that the voltage drop can be measured but short enough so that the voltage at the CUT is still reasonably close to the nominal value at which I_DDOQ is to be measured.

**3.4 Design and Operation of ΔI_DDOQ BICS**

The proposed BICS is shown in Figure 3.10 which is based on the Keating-Mayer concept [12]. Figure 3.9 shows two discharging scenarios. After applying an input voltage to the CUT as shown in Figure 3.10 and after opening the switch, the supply
voltage $V_{DD}$ decreases until it reaches the reference voltage $V_{REF}$. The expression associated with this discharge is given by,

$$I_{DDQ} = C \left( \frac{\Delta V}{\Delta t} \right)$$  \hspace{1cm} (3.3)

where $\Delta V = V_{DD} - V_{REF}$ and $C$ is the circuit capacitance. The time, $\Delta t$, which takes the discharging voltage to reach $V_{REF}$ is measured by a counter, as ‘m’ period of the clock frequency, $T_{CLK}$. By replacing $\Delta t$ by $m \times T_{CLK}$, we obtain the following expression,

$$m = \frac{(C/I_{DDQ}) \Delta V f_{CLK}}{f_{CLK}}$$  \hspace{1cm} (3.4)

In Eq. (3.4), the number ‘m’ of counter counts is inversely proportional to $I_{DDQ}$ and directly proportional to $C$, $\Delta V$ and $f_{CLK}$. From Eq. (3.4) an important observation can be made, that is, if the $I_{DDQ}$ current is less, the discharge time is increased which results in increased ‘m’.

### 3.4.1 The $\Delta I_{DDQ}$ BICS Circuit Design

The BICS as shown in Figure 3.10 consists of four parts, the switching part, the capacitor part, the analog comparator and the counter part. Initially the power supply is given to the CUT through a switch (TG1), another switch TG2 which is between CUT and BICS separates the BICS from the CUT. During this period, capacitor($C$) is charged. Now when the switch (TG1) is off, the capacitor discharges through the CUT and this discharging voltage is compared to a reference voltage using an analog comparator and gives a pulse as output. This pulse output is given as an input to the counter with a fixed clock pulse, which counts the number of counts in the period of the pulse. Now if initially there is no fault induced in the CUT, fault free $I_{DDQ}$ current will be shown as a pulse of certain time period at the output of analog comparator and the counter output will have a count corresponding to that which is taken as reference. In presence of any fault in the circuit, the pulse output varies and the count will be different to that of the reference
Figure 3.8: $I_{DDQ}$ current measurement using power supply measurement [12].
Figure 3.9: Two varying discharge paths.
Figure 3.10: Design of the $\Delta I_{DDQ}$ BICS along with CUT.
count. The switches are designed using a transmission gates, the capacitor (C) is 500 fF and is designed in such a way that there is enough discharge to measure the total fault free and faulty currents and at the same time it should be large enough to avoid parasitic capacitances. The analog comparator is basically a differential amplifier. The counter in Figure 3.10 is a 4-bit binary synchronous counter. The BICS of Figure 3.10 has a resolution of 0.5 µA. This indicates that the BICS is capable of detecting $I_{DDQ}$ currents with a variation of 0.5 µA.

### 3.4.2 Comparator Design

Figure 3.11 shows the CMOS circuit diagram of a comparator. Transistors M1, M2 constitute the simple n-channel differential stage with M3, M4 as current source loads. Transistors M5, M6 and M7 constitute the double ended to single ended conversion stage. Transistors M8-M9, M10-M11, M12- M13 constitute three inverters which act as buffer for the output stage. For operation of the circuit, for example consider the case in which $V_{NEG}$ is 1V input and $V_{POS}$ is a discharging input starting from 2.5V. Initially when $V_{NEG}$ is 1V and $V_{POS}$ is 2.5V, the current that is drawn by M1 is less compared to current that goes through M2 because of the voltage drop across M1 which is less than that of M2. As a result less current diverts to the double ended to single ended stage from the node N2 than from the node N1. This leads to switching of M6 which results in a very low output voltage and is less than the threshold of the following inverter (Inv1). As a result the output of this inverter (Inv1) is 1V which finally leads to 2.5V at the $V_{OUT}$. Now this situation continues as long as the $V_{POS}$ is above 1V. As soon as it reaches 1V the current diverted from N2 to node N also increases such that the input voltage to the first inverter stage (Inv1) is increased to more than the threshold voltage of n-MOS of the inverter which results in 0 V at the output of the inverter (Inv1) and further results in
Figure 3.11: Comparator design.
3.4.3 Synchronous Binary Counter Design

Figure 3.12 shows the design of a 4-bit synchronous binary counter. To determine the gates required at each flip-flop input, let's start by drawing up a truth table for all states of the counter. The truth table is shown in Table 3.1. Looking first at the output of the flip-flop (A), we note that it must change state with every input clock pulse. Therefore, we use J-K flip-flop with both J and K inputs of the flip-flop connected to logic ‘1’ in order to get the correct activity. In order to have all the stages of the counter same we use J-K flip-flops for the rest of the stages with both J and K inputs connected together. Flip-flop (B) is a bit more complicated. This output must change state only on every other input clock pulse. Looking at the truth table again, output B must be ready to change states whenever output A is logic ‘1’, but not when output of A is logic ‘0’. If we recall the behavior of the J-K flip-flop, we can see that if we connect output A to the J and K inputs of flip-flop B, we will see that output B behaves correctly. Continuing this line of reasoning, output C may change state only when both A and B are logic ‘1’. We can't use only output B as the control for flip-flop C; that will allow C to change state when the counter is in count state 2 (0010), causing it to switch directly from a count of 2 (0010) to a count of 7 (0111), and again from a count of 10 (1010) to a count of 15 (1111), the simple reason for the irregular change of states being that the J-K flip-flop changes state whenever input is logic ‘1’. Therefore, we will need a two-input AND gate at the input of flip-flop (C). The inputs of the two-input AND gate are outputs of flip-flop (A) and flip-flop (B) so that flip-flop (C) changes state only when both the outputs of A and B are logic ‘1’. Flip-flop D requires a three-input AND gate for its control, as outputs A, B, and
Figure 3.12: A 4-bit synchronous binary counter

Table 3.1. Truth table of a 4-bit synchronous binary counter.

<table>
<thead>
<tr>
<th>States</th>
<th>Counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>D C B A</td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>2</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>3</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>4</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>5</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>6</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>7</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>8</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>9</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>10</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>11</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>12</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>13</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>14</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>15</td>
</tr>
</tbody>
</table>
C must all be at logic ‘1’ before D can be allowed to change state.

3.4.4 Operation of Proposed $\Delta I_{DDQ}$ BICS

Figure 3.13 shows the operation of the BICS. As can be seen from Figure 3.13, the CUT is connected to the power supply through a switch which is a transmission gate TG1, whose input is ‘$V_{TG}$’ which is a short pulse of duration 1µs. So initially when the switch is on for a short duration the capacitor ‘C’ gets charged. At this time the CUT is disconnected from the BICS by using second transmission gate TG2 who’s ON and OFF times are exactly the reverse of the TG1. Now when the switch is OFF after a short duration, the CUT gets connected to the BICS through the second transmission gate. During this time the capacitor ‘C’ discharges through the CUT and this discharging voltage appears as one of the inputs to the comparator. Initially when there is no fault introduced into the CUT, we get an output of certain duration from the analog comparator depending upon the $V_{REF}$ which is the reference voltage given at the negative terminal of the comparator. The pulse output is given as an input to the 4-bit synchronous binary counter which counts the number of counts for the duration of the pulse as shown in Figure 3.10. This number of counts is taken as a reference. So when a fault is introduced in the CUT, the pulse output varies due to variation in the discharge from that obtained when there is no fault. This gives a different number of counts when compared to the reference counts with no fault. In designing the counter, care must be taken to see that the counter frequency must be sufficiently large enough so that faults with slight variation in the pulse width don’t count the same number of counts as the reference count.

3.5 Faults Introduction into BICS

The faults are introduced in the design using a fault-injection transistor (FIT) [27].
Figure 3.13: Circuit showing BICS operation.
There are a total of five bridging faults introduced in the design and are tested. Activating the fault-injection transistor activates the fault. The use of fault-injection transistor for the fault simulation prevents permanent damage to the 12-bit DAC by just introduction of a metal short. This enables the operation of the DAC without any observable performance degradation in its normal mode of operation. Figure 3.14(a) shows the fault injection transistor in an n-MOSFET. To create an internal bridging fault, the fault-injection transistor is connected to opposite potentials. When the gate of the fault-injection transistor \( V_E \) is connected to \( V_{DD} \), a low resistance path is created between its drain and source nodes and a path from \( V_{DD} \) to GND is formed. In the Figure 3.14(b), an internal bridging fault is created in the CMOS inverter between the drain and source nodes using the fault-injection transistor. When logic ‘0’ is applied at the input of the inverter, the output of the inverter is at logic ‘1’ or \( V_{DD} \). When logic ‘1’ is applied to the gate (\( V_E \)) of the n-MOS FIT, it turns on and this causes a low resistance path between the output of the inverter and the \( V_{SS} \) (GND). This gives rise to an excessive \( I_{DDQ} \) current providing an extra path from \( V_{DD} \) to GND and this can be detected by the BICS.

There are total of five faults introduced using the n-MOS FITs. The n-MOS FIT is designed for \( W/L \) of 1.05/0.6. The FITs are activated externally using error signals \( V_{E1}, V_{E2}, V_{E3}, V_{E4} \) and \( V_{E5} \), respectively. Error signal \( V_{E1} \) is applied to the gate of the FIT in defect 1, which forms a short between the gate and source in the multiplexer circuit shown in Figure 3.15. Error signals \( V_{E2} \) and \( V_{E3} \) are applied to the gates of FITs in defect 2 and defect 3, respectively. Defect 2 forms a short between the drain and source and defect 3 forms a short between drain and gate in the operational amplifier circuit shown in Figure 3.16. Error signals \( V_{E4} \) and \( V_{E5} \) are applied to the gates of FITs in defect 4 and defect 5, respectively. Defect 4 forms a short between source and substrate and defect 5
forms an integrated short in the unit gain operational amplifier circuit shown in Figure 3.17.

### 3.6 Design Specifications of the BICS Used for Testing of 12-Bit DAC

The layout of the $\Delta I_{DDQ}$ BICS is shown in Figure 3.18. The Overall layout of the BICS along with 12-bit DAC is shown in Figure 3.19. The capacitance used to discharge through the CUT is designed to be 500 fF, large enough to avoid parasitic capacitances but at the same time good enough to provide variable discharges with and without faults.

There are two transmission gates acting as switches. TG1 is used to switch the power supply ON and OFF and TG 2 is used to connect the CUT to the BICS during the testing mode and disconnect by switching it OFF during the normal mode of operation of the DAC. The comparator used is designed to act properly with a $V_{REF}$ signal at the negative terminal as 1V. For no fault condition, the output pulse is 51 $\mu$s for no fault condition. This pulse width is sufficiently large enough to allow large $I_{DDQ}$ pulse output variations (caused due to some faults) to fall within this pulse width. The no fault condition pulse output and the variation of pulse outputs due to faults introduced by error signals $V_{E1}$, $V_{E2}$, $V_{E3}$, $V_{E4}$ and $V_{E5}$ of Figures 3.15, 3.16, 3.17 are shown in Figures 3.20, 3.21, 3.22, 3.23, 3.24, 3.25 respectively. The counter designed is a 4-bit synchronous binary counter with time period of 5 $\mu$s (frequency of 200 KHz). Count for the no fault condition is ‘1010’ (10 in decimal). This is shown in Figure 3.26. The total available chip area is $897 \times 897 \mu$m$^2$ on a tiny chip. The DAC occupies $504 \times 501 \mu$m$^2$ area of the chip. The BICS occupies $498 \times 75 \mu$m$^2$ area of the chip which is 5.1% of the total chip area.
Figure 3.14: (a) Fault-injection transistor (FIT).

Figure 3.14: (b) Fault-injection transistor between drain and source nodes of a CMOS inverter.
Figure 3.15: Multiplexer circuit with defect-1 activated from $V_{E1}$. 
Figure 3.16: Operational amplifier showing drain-source and drain-gate shorts.
Note: For the P-MOSFETS the substrate is connected to $V_{DD}$. 
Figure 3.17: Unit gain amplifier showing source-substrate and inter-gate shorts. Note: For the P-MOSFETS the substrate is connected to $V_{DD}$. 
Figure 3.18: $\Delta I_{DDQ}$ BICS layout.
Figure 3.19: Chip layout integrating $\Delta I_{DDQ}$ BICS and 12-bit CMOS DAC.
Figure 3.20: Post layout simulation of the comparator with no fault.
Figure 3.21: Post layout simulation of the comparator with defect-1.
Figure 3.22: Post layout simulation of the comparator with defect-2.
Figure 3.23: Post layout simulation of the comparator with defect-3.
Figure 3.24: Post layout simulation of the comparator with defect-4.
Figure 3.25: Post layout simulation of the comparator with defect-5.
Figure 3.26. Post layout simulations of the integrated BICS and the 12-bit DAC showing comparator output, clock pulse to counter and outputs of counter from LSB ($V_A$) to MSB ($V_D$).
CHAPTER 4

THEORETICAL AND EXPERIMENTAL RESULTS

This chapter discusses the theoretical and experimental results of the $\Delta I_{DDQ}$ testing for a 12-bit charge scaling DAC. The theoretical results are obtained from the post-layout PSPICE (PSpice A/D Simulator, V.10.1) simulations. MOSIS BISM3 model parameters [33] are used which are summarized in Appendix A. The chip was designed using L-EDIT, V.10.20 in standard 0.5 $\mu$m n-well CMOS technology. The total available chip area is $897 \times 897$ $\mu$m$^2$ on a tiny chip. The DAC occupies $504 \times 501$ $\mu$m$^2$ area of the chip. The BICS occupies $498 \times 75$ $\mu$m$^2$ area of the chip which is 4.6% of the total chip area. HP 1660CS Logic Analyzer was used for testing the packaged device described in Appendix B.

4.1 Simulation and Measured Results

Figure 4.1 shows the layout of a 12-bit charge scaling digital-to-analog converter with five fault injection transistors distributed across the chip. FIT-1 is induced in the multiplexer part of the chip, FIT-2 and FIT-3 in the operational amplifier part of the chip and FIT-4 and FIT-5 are induced in the sample and hold part the chip. Figure 4.2 shows the chip layout of a 12-bit charge scaling DAC including BICS within a pad frame of 1.154 mm $\times$ 1.154 mm size. Figure 4.3 shows the microchip photograph of 12-bit charge scaling showing the BICS (bordered) and DAC as the rest of the part. Figure 4.4 shows the simulated and measured output characteristics of the 12-bit charge scaling DAC when the faults are not activated. The equivalent analog output voltage is shown for some of the input voltages among 4096 input combinations of the DAC. Figure 4.5 shows the measured DNL characteristics of the 12-bit charge scaling DAC when the faults are not
Figure 4.1: CMOS chip layout of a 12-bit charge scaling DAC with five fault injection transistors distributed across the chip.
Figure 4.2: Tiny CMOS chip layout of a 12-bit charge scaling DAC including BICS within a padframe of 1.154 mm × 1.154 mm size.
Figure 4.3: Microchip photograph of the 12-bit charge scaling DAC and BICS for $\Delta I_{DDQ}$ testing.
Figure 4.4: Simulated and measured characteristics of a 12-bit charge scaling DAC.
activated. DNL is within ±0.7 LSB. Figure 4.6 shows the measured INL characteristics of the 12-bit charge scaling DAC when the faults are not activated. INL is less than ±1 LSB.

Figure 4.7 shows the simulated output of the op-amp when the fault (VE3) is activated (Fig 3.16). When the op-amp is given a 50 KHz sine wave of 0.9V, the output obtained is a sine wave of 100 mV with a gain of 0.1. Figure 4.8 shows the gain versus frequency response of the op-amp with fault activated. The amplifier 3 dB gain with the fault activated is 16 dB as compared to 28 dB when the fault is deactivated. The bandwidth is increased to 20 MHz from 40 KHz without fault (Fig 2.29).

The reference voltage of the analog comparator is 1 V. The simulated power discharge along with the comparator pulse output for the case when there is no fault induced is shown in Figure 4.9. The simulated pulse width is 51 μs and the corresponding measured value is 49.6 μs as observed in Figure 4.10. Figure 4.11 shows the simulated output of the comparator and the counter count which is 10 clock pulses (1010) for the fault free condition. Measured counter count is shown in Figure 4.12 and is obtained from HP 1660CS Logic Analyzer. Total five bridging faults have been induced into the DAC. The first fault FIT-1 activated by the error signal VE1 is at the multiplexer part (Fig 3.15). The counter count for this case is one (0001). The simulated output is shown in Figure 4.13 and the corresponding measurements in Figure 4.14. The second fault FIT-2 activated by error signal VE2 is at the operational amplifier part (Figure 3.16) and it is a drain-source short. The counter count for this case is 14 (1110). The simulated output is shown in Figure 4.15 and the experimental results in Figure 4.16. The third fault FIT-3 activated by error signal VE3 is also in the operational amplifier part (Fig 3.16) and it is a drain-gate short. The counter count for this case is 9(1001). The simulated output is
Figure 4.5: Measured DNL characteristics of a 12-bit charge scaling DAC.
Figure 4.6: Measured INL characteristics of a 12-bit charge scaling DAC.
Figure 4.7: Voltage gain response of op-amp with fault introduced.
Note: Input is applied at the non-inverting input.
Figure 4.8: Gain versus frequency response of the CMOS op-amp circuit with fault Introduced.
Figure 4.9: Simulated comparator input and output for the fault free condition.
Figure 4.10: Measured comparator input and output for fault free condition. Scale: X-axis: 20 µs/div and Y-axis: 1V/div.
Figure 4.11: Simulated output of the comparator and the counter count for the fault free condition.
Figure 4.12: Measured output of the comparator and the counter count for the fault free condition obtained from HP 1660cs Logic Analyzer.
Figure 4.13: Simulated output of the comparator and the counter count for FIT-1
Figure 4.14: Measured output of the comparator and the counter count for FIT-1.
Figure 4.15: Simulated output of the comparator and the counter count for FIT-2.
Figure 4.16: Measured output of the comparator and the counter count for FIT-2.
shown in Figure 4.17 and the experimental results in Figure 4.18. The fourth fault FIT-4 is activated by the error signal $V_{E4}$ is at the sample and hold part of the circuit (Fig 3.17) and it is a source-substrate short. The counter count for this case is 2 (0010). The simulated output is shown in Figure 4.19 and the corresponding experimental results in Figure 4.20. The fifth fault FIT-5 is activated by the error signal $V_{E5}$ is also at the sample and hold part of the circuit (Figure 3.18) and it is an inter-gate short. The counter count for this case is 8 (0111). The simulated output is shown in Figure 4.21 and the experimental results in Figure 4.22. Table 4.1 summarizes simulated and measured $I_{DDQ}$ and output pulse width values for comparison for five induced faults and the fault free condition. The BICS in the present design can differentiate $I_{DDQ}$ with a difference of 0.5 μA.
Table 4.1 Fault and fault free current and pulse width

<table>
<thead>
<tr>
<th>Faults</th>
<th>Current (µA) (Sim)</th>
<th>Pulse Width (µs) (Sim)</th>
<th>Current (µA) (Measured)</th>
<th>Pulse Width (µs) (Measured)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault Free</td>
<td>19</td>
<td>51</td>
<td>19.2</td>
<td>49.6</td>
</tr>
<tr>
<td>Fault 1 (FIT-1)</td>
<td>22</td>
<td>5.2</td>
<td>22.2</td>
<td>4.5</td>
</tr>
<tr>
<td>Fault 2 (FIT-2)</td>
<td>15</td>
<td>70</td>
<td>15.3</td>
<td>68.6</td>
</tr>
<tr>
<td>Fault 3 (FIT-3)</td>
<td>19.5</td>
<td>47.5</td>
<td>19.7</td>
<td>46.2</td>
</tr>
<tr>
<td>Fault 4 (FIT-4)</td>
<td>21</td>
<td>13.5</td>
<td>21.2</td>
<td>12.0</td>
</tr>
<tr>
<td>Fault 5 (FIT-5)</td>
<td>20.5</td>
<td>39</td>
<td>20.7</td>
<td>38.6</td>
</tr>
<tr>
<td>All Faults Activated</td>
<td>26</td>
<td>1.5</td>
<td>26.5</td>
<td>0.5</td>
</tr>
</tbody>
</table>
Figure 4.17: Simulated output of the comparator and the counter count for FIT-3.
Figure 4.18: Measured output of the comparator and the counter count for FIT-3.
Figure 4.19: Simulated output of the comparator and the counter count for FIT-4.
Figure 4.20: Measured output of the comparator and the counter count for FIT-4.
Figure 4.21: Simulated output of the comparator and the counter count for FIT-5.
Figure 4.22: Measured output of the comparator and the counter count for FIT-5.
Figure 4.23: Simulated output of the comparator and the counter count for all faults activated.
Figure 4.24: Measured output of the comparator and the counter count for all faults activated.
CHAPTER 5
CONCLUSION

5.1 Conclusion and Scope of Future Work

A 12-bit charge-scaling DAC using split array architecture along with a $\Delta I_{\text{DDQ}}$ BICS based on power discharge phenomenon are designed in standard 0.5 $\mu$m n-well CMOS technology. The DAC is verified experimentally with the simulated values for most of the 4096 digital input word combinations. The unit step is about 0.5 mV. DAC operates with 0 to 2.5 V supply voltages. The reference voltage used is 2 V for a HIGH and GND (0 V) for a LOW. The 12-bit DAC is used as a circuit under test (CUT). The CUT is tested with a $\Delta I_{\text{DDQ}}$ built-in current sensor (BICS), which has a negligible impact on the performance of the circuit under test.

The present BICS works in two-modes: normal mode and the test mode. In the normal mode, BICS is isolated from the CUT due to which there is no performance degradation of the circuit under test. In the testing mode, BICS detects the abnormal current caused by permanent manufacturing defects. The present BICS is designed with a switch (transmission gate), capacitor, analog comparator and a 4-bit counter. The present BICS design is very effective in detecting a small $I_{\text{DDQ}}$ which is normally missed by conventional $I_{\text{DDQ}}$ circuits designed using current mirrors. The BICS can also be applied in testing of several other types of data converter circuits. Apart from these the method can be very effectively applied to any digital VLSI circuits.

The design can be made robust by making the BICS sensitive to process variations which is one of the important factor to be considered in the submicron technology. In submicron CMOS technologies, the rate of discharge for the chip after
fabrication may vary considerably when compared to the simulated discharge. In that case we can internally generate the clock for the counter of the present BICS. This can be achieved by a ring oscillator. Due to process variations if there is any change in the discharge there could be a proportional change in the ring oscillator frequency which compensates for the change in the capacitor discharge by keeping the number of counts of the counter same for the fault free condition.
REFERENCES


IEEE Transactions on Circuits and Systems-II Analog and Digital Signal


[31] B. Kruseman, “Comparison of defect detection capabilities of current-based test

[32] J. R. Vázquez and J. P. de Gyvez, “Built-in current sensor for ΔI\textsubscript{DDQ} testing,”

APPENDIX A

SPICE BSIM3 MOS MODEL PARAMETERS [34]

Model Parameters for n-MOS Transistors

```
.MODEL NMOS NMOS     LEVEL  = 7
+VERSION = 3.1    TNOM    = 27    TOX     = 1.42E-8
+XJ      = 1.5E-7    NCH     = 1.7E17    VTH0    = 0.5873345
+K1      = 0.9230324    K2     = -0.1047761    K3    = 22.4916147
+K3B     = -9.1266087    W0      = 1E-8    NLX     = 2.000399E-9
+DVT0W   = 0    DVT1W    = 0    DVT2W   = 0
+DVT0    = 2.2994082    DVT1    = 0.4970166    DVT2   = -0.1842143
+U0      = 446.7488201    UA     = 1E-13    UB      = 1.299367E-18
+UC      = 1.248923E-13    VSAT    = 1.59167E5    A0     = 0.6101847
+AGS     = 0.1302919    B0      = 2.533749E-6    B1     = 5E-6
+KETA    = -1.666578E-3    A1     = 3.485566E-4    A2    = 0.3674233
+RDSW    = 1.368085E3    PRWG    = 0.0600883    PRWB   = 0.0171806
+WR      = 1    WINT     = 2.09488E-7    LINT    = 7.220693E-8
+XL      = 1E-7    XW      = 0    DWG     = 2.605489E-9
+DWB     = 4.277159E-8    VOFF    = -0.0115079    NFACTOR = 0.7015054
+CIT     = 0    CDSC     = 2.4E-4    CDSCD   = 0
+CDSCB   = 0    ETA0     = 0.0031556    ETAB    = -4.218915E-3
+DSUB    = 0.4129659    PCLM    = 2.4387548    PDIBLC1 = 1
+PDIBLC2  = 4.31964E-3    PDIBLCB = 0.053704    DROUT   = 0.9257597
+PSCBE1   = 6.241157E8    PSCBE2  = 1.459532E-4    PVAG    = 0
+DELTA   = 0.01    RSH     = 83.1    MOBMOD  = 1
+PRT     = 0    UTE      = -1.5    KT1     = -0.11
+KT1L    = 0    KT2     = 0.022    UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0    WLN      = 1    WW      = 0
+WWN     = 1    WWL     = 0    LL      = 0
+LLN     = 1    LW      = 0    LWN     = 1
+LWL     = 0    CAPMOD   = 2    XPART   = 0.5
+CGDO    = 1.92E-10    CGSO    = 1.92E-10    CGBO    = 1E-9
+CI      = 4.303837E-4    PB     = 0.9074906    MJ     = 0.4317275
+CJSW    = 3.001226E-10    PBSW    = 0.8    MJSW   = 0.1714547
+CJSWG   = 1.64E-10    PBSWG   = 0.8    MJSWG  = 0.1714547
+CF      = 0    PVTH0   = 0.0628352    PRDSW   = 346.0290637
+PK2     = -0.0296479    WKETA   = -0.0177686    LKETA   = -2.260032E-3
)```

Model Parameters for p-MOS transistors

```
.MODEL PMOS PMOS     LEVEL  = 7
+VERSION = 3.1    TNOM    = 27    TOX     = 1.42E-8
```

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Mosis Fabricated Chip Model Parameters (T5BK)

Model Parameters for n-MOS Transistors.

.MODEL NMOS NMOS  LEVEL  = 7
 +VERSION = 3.1  TNOM = 27  TOX = 1.4E-8
 +XJ = 1.5E-7  NCH = 1.7E17  VTH0 = -0.9286607
 +K1 = 0.5412389  K2 = 0.0128372  K3 = 11.1025735
 +K3B = -0.8099316  W0 = 3.891267E-7  NLX = 1.278268E-8
 +DVT0W = 0  DVT1W = 0  DVT2W = 0
 +DVT0 = 2.2645652  DVT1 = 0.7212046  DVT2 = -0.1560945
 +U0 = 200.0599104  U = 2.439885E-9  UB = 1.928396E-21
 +UC = -7.00689E-11  VSAT = 1.808499E5  A0 = 0.9334131
 +AGS = 0.1371285  B0 = 2.423807E-7  B1 = 1.124249E-6
 +KETA = -2.535624E-3  A1 = 9.577499E-5  A2 = 0.3
 +RDSW = 3E3  PRWG = 0.0148859  PRWB = -0.0125106
 +WR = 1  WINT = 2.409073E-7  LINT = 8.424942E-8
 +XL = 1E-7  XW = 0  DWG = -1.818861E-9
 +DWB = 2.399629E-8  VOFF = -0.0801078  NFACTOR = 0.4609732
 +CIT = 0  CDSC = 2.4E-4  CDSCD = 0
 +CDSCB = 0  ETA0 = 0.0372311  ETAB = -0.0981321
 +DSUB = 1  PCLM = 2.1048606  PDIBLC1 = 0.0586727
 +PDIBLC2 = 3.988846E-3  PDIBLCB = -0.0530319  DROUT = 0.2623986
 +PSCBE1 = 5.313202E9  PSCBE2 = 5E-10  PVAG = 0
 +DELT = 0.01  RSH = 105.2  MOBMOD = 1
 +PRT = 0  UTE = -1.5  KT1 = -0.11
 +KT1L = 0  KT2 = 0.022  UA1 = 4.31E-9
 +UB1 = -7.61E-18  UC1 = -5.6E-11  AT = 3.3E4
 +WL = 0  WLN = 1  WW = 0
 +WWN = 1  WWL = 0  LL = 0
 +LNN = 1  LW = 0  LWN = 1
 +LWL = 0  CAPMOD = 2  XPART = 0.5
 +CGDO = 2.28E-10  CGSO = 2.28E-10  CGBO = 1E-9
 +CJ = 7.334167E-4  PB = 0.9498634  MJ = 0.4952447
 +CJSW = 2.898167E-10  PBSW = 0.99  MJSW = 0.3046906
 +CJSWG = 6.4E-11  PBSWG = 0.99  MJSWG = 0.3046906
 +CF = 0  PVTH0 = 5.98016E-3  PRDSW = 14.8598424
 +PK2 = 3.73981E-3  WKETA = 8.333721E-3  LKETA = -6.867545E-3 )
\textbf{Model Parameters for p-MOS Transistors.}

\texttt{.MODEL PMOS PMOS LEVEL = 7}
\texttt{+VERSION = 3.1 TNOM = 27 TOX = 1.4E-8}
\texttt{+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.926911}
\texttt{+K1 = 0.5574581 K2 = 7.700848E-3 K3 = 10.5449255}
\texttt{+K3B = -1.1490152 W0 = 1E-8 NLX = 1.199667E-7}
\texttt{+DVT0 = 0 DVT1W = 0 DVT2W = 0}
\texttt{+DVT0 = 2.3955399 DVT1 = 0.5083675 DVT2 = -0.0995504}
\texttt{+U0 = 197.8692907 UA = 2.303168E-9 UB = 1.004803E-21}
\texttt{+UC = -6.86513E-11 VSAT = 1.752687E5 A0 = 0.8562827}
\texttt{+AGS = 0.1323854 B0 = 9.73985E-7 B1 = 5E-6}
\texttt{+KETA = -2.52096E-3 A1 = 5.716175E-4 A2 = 0.3009519}
\texttt{+RDSW = 3E3 PRWG = -0.0410649 PRWB = -0.0209007}
\texttt{+WR = 1 WINT = 2.429516E-7 LINT = 1.03343E-7}
\texttt{+XL = 1E-7 XW = 0 DWG = 9.457803E-11}
\texttt{+DWB = 2.0427E-8 VOFF = -0.064019 NFACTOR = 0.781202}
\texttt{+CIT = 0 CDSC = 2.4E-4 CDSCD = 0}
\texttt{+CDSCB = 0 ETA0 = 0.5092897 ETAB = -0.0772273}
\texttt{+DSUB = 1 PCLM = 2.177819 PDIBLC1 = 0.0235286}
PDIBLC2 = 3.323759E-3    PDIBLCB = -0.0555775    DROUT = 0.1538436
PSCBE1 = 7.500246E9    PSCBE2 = 7.086397E-10    PVAG = 0
DELTAL = 0.01    RSH = 103.5    MOBMOD = 1
PSCBE1 = 7.500246E9    PSCBE2 = 7.086397E-10    PVAG = 0
DELTA = 0.01    RSH = 103.5    MOBMOD = 1
PRT = 0    UTE = -1.5    KT1 = -0.11
KT1L = 0    KT2 = 0.022    UA1 = 4.31E-9
UB1 = -7.61E-18    UC1 = -5.6E-11    AT = 3.3E4
WL = 0    WLN = 1    WW = 0
WLN = 1    WWL = 0    LL = 0
LLN = 1    LW = 0    LWN = 1
CAPMOD = 2    XPART = 0.5
CGDO = 2.36E-10    CGSO = 2.36E-10    CGBO = 2E-9
CJ = 7.269409E-4    PB = 0.9619968    MJ = 0.5005182
CJSW = 2.878663E-10    PBSW = 0.99    MJSW = 0.3108389
CJSWG = 6.4E-11    PBSWG = 0.99    MJSWG = 0.3108389
CF = 0    PVTH0 = 5.98016E-3    PRDSW = 14.8598424
PK2 = 3.73981E-3    WKETA = 4.744039E-3    LKETA = -2.576487E-3 }
APPENDIX B

CHIP TESTABILITY

Figure B.1 shows the 12-bit DAC with BICS in 1.5 mm \( \times \) 1.5 mm padframe. Figure B.2 shows the microchip photograph of 12-bit DAC with \( \Delta I_{DDQ} \) BICS. The design includes individual sub-modules for testing the device.

B.1 Inverter Module and Testing

Table B.1

<table>
<thead>
<tr>
<th>PIN No.</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>34</td>
<td>Input</td>
</tr>
<tr>
<td>35</td>
<td>Output</td>
</tr>
</tbody>
</table>

DC test was performed on the independent inverter module to test if the chip did not have fabrication problems. Logic ‘0’ is applied at the input pin #34 and output (logic ‘1’) is observed on pin #35. Logic ‘1’ is applied at the input pin #34 and output (logic ‘0’) is observed on pin #35. Table B.1 describes the I/O pins of the test inverter.

B.2 12-bit DAC with \( \Delta I_{DDQ} \) BICS and Testability

Table B.2 gives the pin numbers and their description to test 12-bit DAC.

Table B.2

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Description of PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D3 (I/p to DAC)</td>
</tr>
<tr>
<td>2</td>
<td>D4 (I/p to DAC)</td>
</tr>
<tr>
<td>3</td>
<td>( V_{SS_DAC} ) (( V_{SS} ) for DAC)</td>
</tr>
<tr>
<td>4</td>
<td>Error_Signal_1</td>
</tr>
<tr>
<td>5</td>
<td>Pin(not considered)</td>
</tr>
<tr>
<td>6</td>
<td>( V_D ) (Counter Output)(MSB)</td>
</tr>
<tr>
<td>7</td>
<td>( V_C ) (Counter Output)</td>
</tr>
<tr>
<td>8</td>
<td>( V_B ) (Counter Output)</td>
</tr>
<tr>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>---</td>
<td>-------------</td>
</tr>
<tr>
<td>9</td>
<td>$V_A$ (Counter Output) (LSB)</td>
</tr>
<tr>
<td>10</td>
<td>Analog Comparator Output</td>
</tr>
<tr>
<td>11</td>
<td>I/p to negative of Comparator</td>
</tr>
<tr>
<td>12</td>
<td>Short Pulse to Transmission Gate switch</td>
</tr>
<tr>
<td>13</td>
<td>Clock Input to Counter</td>
</tr>
<tr>
<td>14</td>
<td>Clear Input to Counter</td>
</tr>
<tr>
<td>15</td>
<td>D5 (I/p to DAC)</td>
</tr>
<tr>
<td>16</td>
<td>D6 (I/p to DAC)</td>
</tr>
<tr>
<td>17</td>
<td>D7 (I/p to DAC)</td>
</tr>
<tr>
<td>18</td>
<td>$V_{DD1}$ (Supply to DAC in normal mode and also pin for testing capacitor discharge path in the testing mode)</td>
</tr>
<tr>
<td>19</td>
<td>$V_{REF}$ (reference voltage input to DAC)</td>
</tr>
<tr>
<td>20</td>
<td>$V_{RESET}$ (reset to charge the capacitors of DAC for a short time)</td>
</tr>
<tr>
<td>21</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>22</td>
<td>D8 (I/p to DAC)</td>
</tr>
<tr>
<td>23</td>
<td>D9 (I/p to DAC)</td>
</tr>
<tr>
<td>24</td>
<td>D10 (I/p to DAC)</td>
</tr>
<tr>
<td>25</td>
<td>D11 (I/p to DAC)</td>
</tr>
<tr>
<td>26</td>
<td>Control I/P to Sample and Hold Circuit</td>
</tr>
<tr>
<td>27</td>
<td>Pin (not Considered)</td>
</tr>
<tr>
<td>28</td>
<td>Pin (not Considered)</td>
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### B.3 12-bit DAC Testing in Normal Mode

1. Supply voltage of 0 to 2.5 V is given to the power supply pin numbers of the chip ($V_{DD} = +2.5V$ and $V_{SS} = 0V$).

2. In order to avoid convergence problem the two circuits, the BICS and the DAC have separate $V_{SS}$. The main $V_{SS}$ at pin (#40) is given to the BICS and another pad at (#3) which is just a input pad is used as $V_{ss}$ for the DAC.

3. The $V_{DD1}$ at pin (#18) is given a ‘high’ voltage (+2.5V), which makes the DAC to function in the normal mode of operation. So $V_{dd1}$ becomes DAC supply in the normal mode.

4. The fault-injection transistors must be de-activated by giving a ‘low’ voltage (0V) to the error-signals $V_{E1}$, $V_{E2}$, $V_{E3}$, $V_{E4}$ and $V_{E5}$.

5. The DAC is tested by giving various combinations of inputs to the digital input pins 37, 38, 39, 1,2,15,16,17,22,23,24,25 with pin (#25) i.e. D11 being the MSB and pin (#37) i.e. D0 being the LSB.

6. $V_{REF}$ at pin (#19) which is the voltage reference for the DAC is given a dc input of 2V.

7. $V_{RESET}$ at pin (#20) which initially charges the capacitor is a short PWL signal with 0 to 2.5V.

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<tr>
<td>29</td>
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<tr>
<td>30</td>
<td>Error_Signal_2</td>
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<td>34</td>
<td>Inverter Input (Test inverter )</td>
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<td>35</td>
<td>Inverter Output (Test Inverter)</td>
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<td>36</td>
<td>DAC Output</td>
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<tr>
<td>37</td>
<td>D0 (I/p to DAC)</td>
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<tr>
<td>38</td>
<td>D1 (I/p to DAC)</td>
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<td>39</td>
<td>D2 (I/p to DAC)</td>
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<tr>
<td>40</td>
<td>$V_{SS}$</td>
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</table>
8. Control input to sample and hold circuit at pin (#26) is a pulse input with 0 to 2.5V

9. Finally the output of the DAC is observed at pin #36 on the oscilloscope.

B.4 $\Delta I_{DDQ}$ Testing of the 12-bit DAC in Test Mode

1. In the test mode the $V_{DD1}$ pin (#18) is left floating which results in the supply line of DAC connected to the input of the BICS.
2. The fault-injection n-MOS transistors are activated one at a time by connecting the error-signals $V_{E1}$, $V_{E2}$, $V_{E3}$ and $V_{E4}$ to a HIGH voltage (+2.5V).
3. The input to the transmission gate (TG) at pin (#12) is a short pulse of duration 0.8 $\mu$s, which is sufficient to charge the capacitor across the CUT.
4. A dc voltage of 1V is given at the negative input of the analog comparator which gives a pulse of 49.6 $\mu$s at the output of the comparator.
5. The clock input to the counter is at pin (#13) whose time period is 5 $\mu$s and the clear input to the counter which is a dc 2.5V is given at pin (#14).
6. The comparator output which is a pulse of certain duration is checked in the oscilloscope at pin (#10).
7. The 4-bit counter outputs $V_A$, $V_B$, $V_C$ and $V_D$ (with $V_A$ and $V_D$ being LSB and MSB respectively) along with the comparator pulse output are observed in the logic analyzer, HP 1660CS.
8. When faults activated one at a time different counts of the counter are observed in the logic analyzer.
Figure: B.1 12-bit DAC with BICS in the 1.5 mm × 1.5 mm padframe.
Figure B.2: Microchip photograph of 12-bit charge scaling DAC and BICS for $\Delta I_{DDQ}$ testing.
VITA

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